

## SEMI F-47 Test Compliance Test Report

### Standard:

**SEMI F47-0200**

**Specification for Semiconductor Processing Equipment**

**Voltage Sag Immunity**

### Test Procedure Standard:

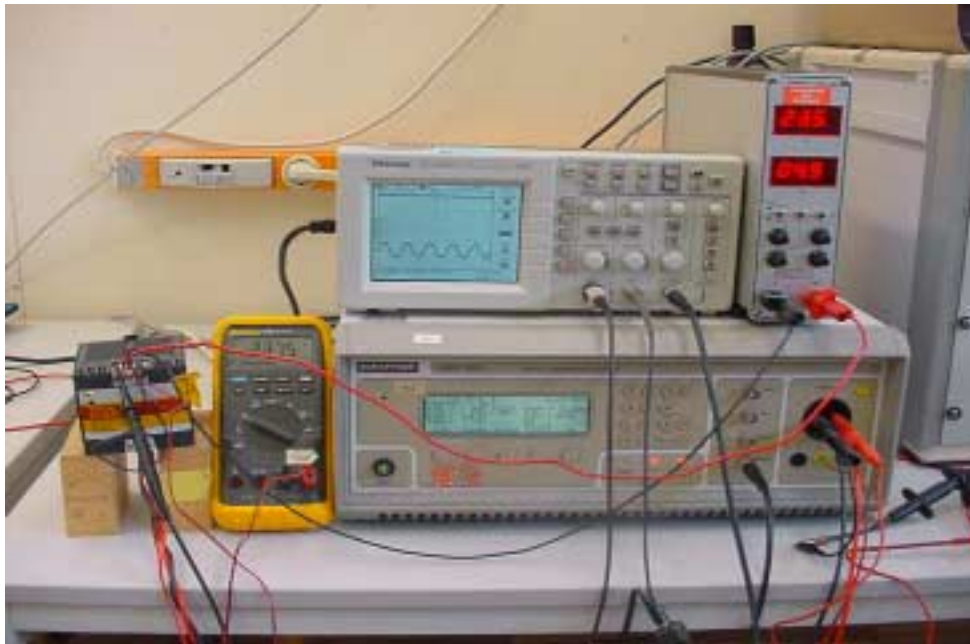
**Semi F42 : Test method for Semiconductor Processing Equipment.**

**Voltage Sag Immunity**

#### 1. Test Setup

Sag Generator: Schaffner NSG1003: Dropout and Variation Simulator

Tektronics: TDS1002



#### 2. Test Units

Units Name	Nominal Voltage [VAC]	Output Voltage [V]	Output Current [A]
TCL24-105	100-240	5	4
TCL24-112	100-240	12	2
TCL24-124	100-240	24	1
TCL060-112	100-240	12	4
TCL060-124	100-240	24	2.5
TCL060-148	100-240	48	1.25
TCL120-112	100-240	12	8
TCL120-124	100-240	24	5

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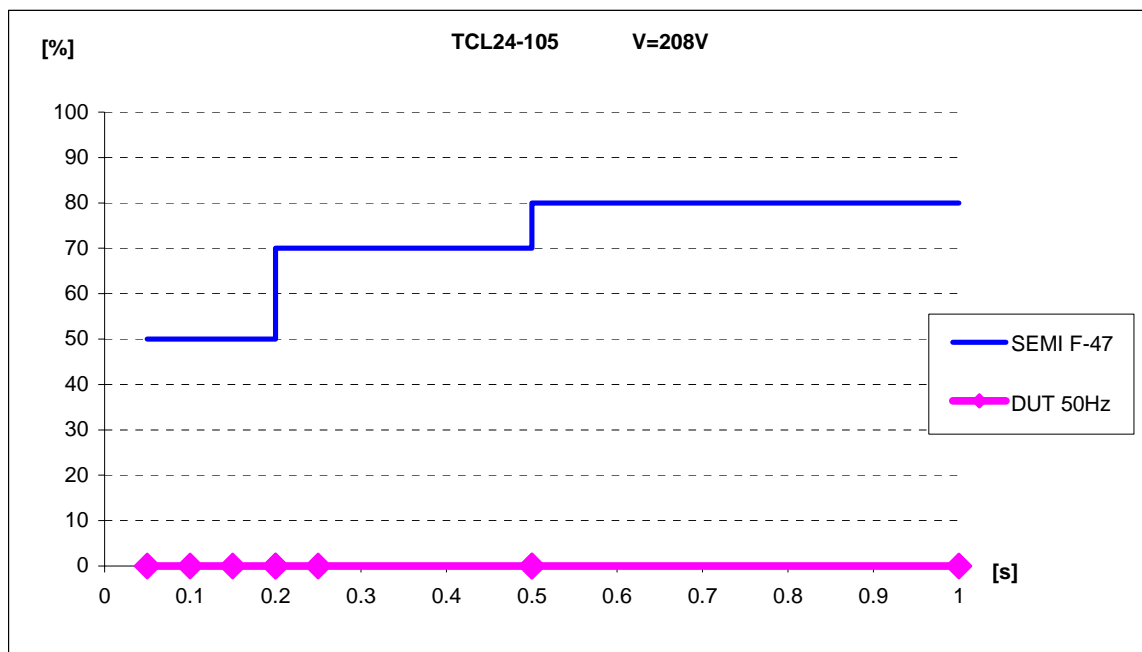
### 3. Test Report

#### 3.1 TCL24-105

Input Voltage V=208VAC

Output: V=5VDC/4A

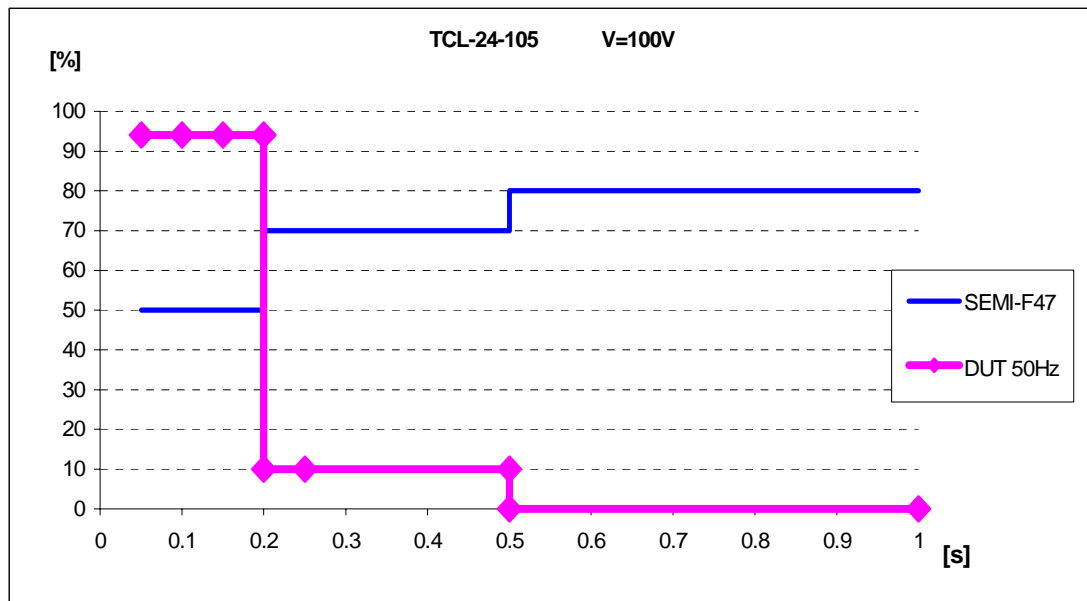
Voltage Sag [V]	Duration		Output Voltage [V]	Percent of Nominal		Result
	[s]	Cycles		DUT 50Hz [%]	SEMI F47 [%]	
166.4	1	50	5	0.0	80	PASS
166.4	0.5	25	5	0.0	80	PASS
145.6	0.5	25	5	0.0	70	PASS
145.6	0.25	12.5	5	0.0	70	PASS
145.6	0.2	12.5	5	0.0	70	PASS
104	0.2	10	5	0.0	50	PASS
104	0.15	7.5	5	0.0	50	PASS
104	0.1	5	5	0.0	50	PASS
104	0.05	2.5	5	0.0	50	PASS
104	0.02	1	5	0.0	50	PASS
0	0.02	1	5	0.0	0	PASS



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**TCL24-105****Input Voltage V=100VAC****Output: V=5VDC/4A**

Voltage Sag [V]	Duration [s]	Cycles	Output Voltage		Percent of Nominal		Result
			[V]		DUT 50Hz [%]	SEMI F47 [%]	
80	1	50	5	0.0	80	80	PASS
80	0.5	25	5	0.0	80	80	PASS
70	0.5	25	4.5	10	70	70	PASS
70	0.25	12.5	4.5	10	70	70	PASS
70	0.2	12.5	4.5	10	70	70	PASS
50	0.2	10	0.3	90	50	50	FAIL
50	0.15	7.5	0.3	90	50	50	FAIL
50	0.1	5	0.3	90	50	50	FAIL
50	0.05	2.5	0.3	90	50	50	FAIL
50	0.02	1	5	0	50	50	PASS
0	0.02	1	5	0	0	0	PASS



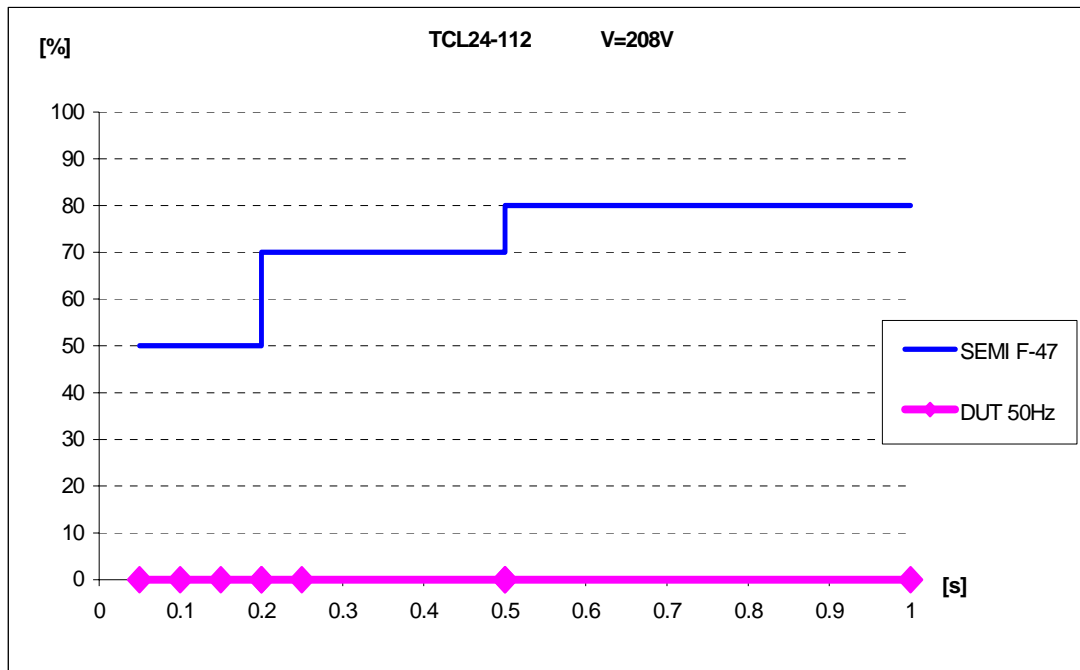
				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
						SEMI F47 Compliance	Sheet/of 3/20
Iss.	Change	Date	Name				

### 3.2 TCL24-112

Input Voltage V=208VAC

Output: V=12VDC/2.0A

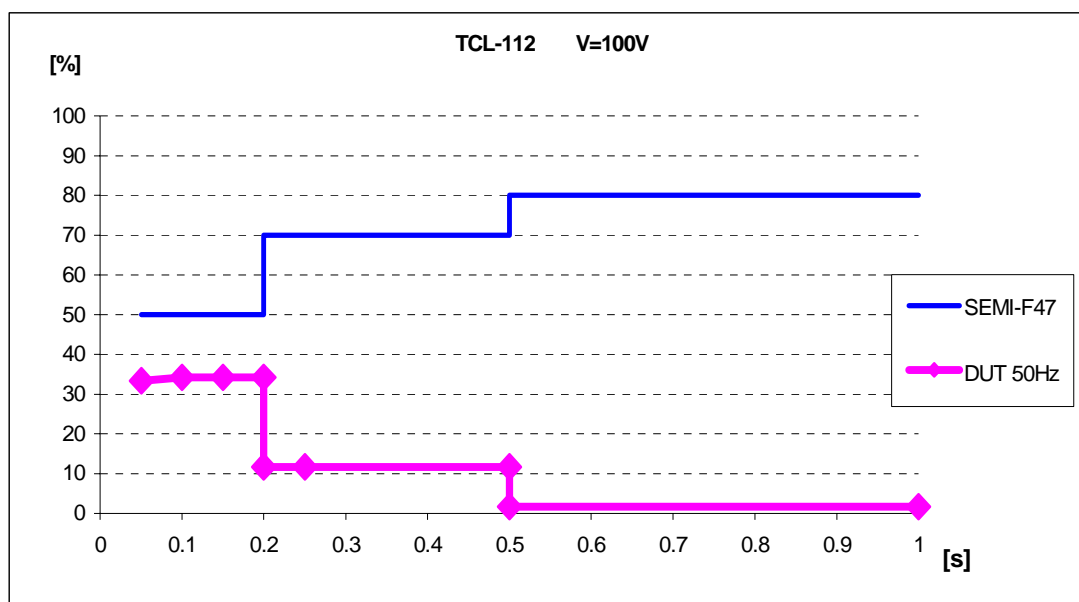
Voltage Sag [V]	Duration		Output Voltage [V]	Percent of Nominal		Result
	[s]	Cycles		DUT 50Hz [%]	SEMI F47 [%]	
166.4	1	50	12	0.0	80	PASS
166.4	0.5	25	12	0.0	80	PASS
145.6	0.5	25	12	0.0	70	PASS
145.6	0.25	12.5	12	0.0	70	PASS
145.6	0.2	12.5	12	0.0	70	PASS
104	0.2	10	12	0.0	50	PASS
104	0.15	7.5	12	0.0	50	PASS
104	0.1	5	12	0.0	50	PASS
104	0.05	2.5	12	0.0	50	PASS
104	0.02	1	12	0.0	50	PASS
0	0.02	1	12	0.0	0	PASS



				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
						SEMI F47 Compliance	Sheet/of 4/20
Iss.	Change	Date	Name				

**TCL24-112**  
**Input Voltage V=100VAC**  
**Output: V=12VDC/2.0A**

Voltage Sag	Duration		Output Voltage	Percent of Nominal		
[V]	[s]	Cycles	[V]	DUT 50Hz [%]	SEMI F47 [%]	Result
80	1	50	11.8	1.7	80	PASS
80	0.5	25	11.8	1.7	80	PASS
70	0.5	25	10.6	11.7	70	PASS
70	0.25	12.5	10.6	11.7	70	PASS
70	0.2	12.5	10.6	11.7	70	PASS
50	0.2	10	7.9	34.2	50	PASS
50	0.15	7.5	7.9	34.2	50	PASS
50	0.1	5	7.9	34.5	50	PASS
50	0.05	2.5	8	33.3	50	PASS
50	0.02	1	10.8	10	50	PASS
0	0.02	1	10.8	10	0	PASS



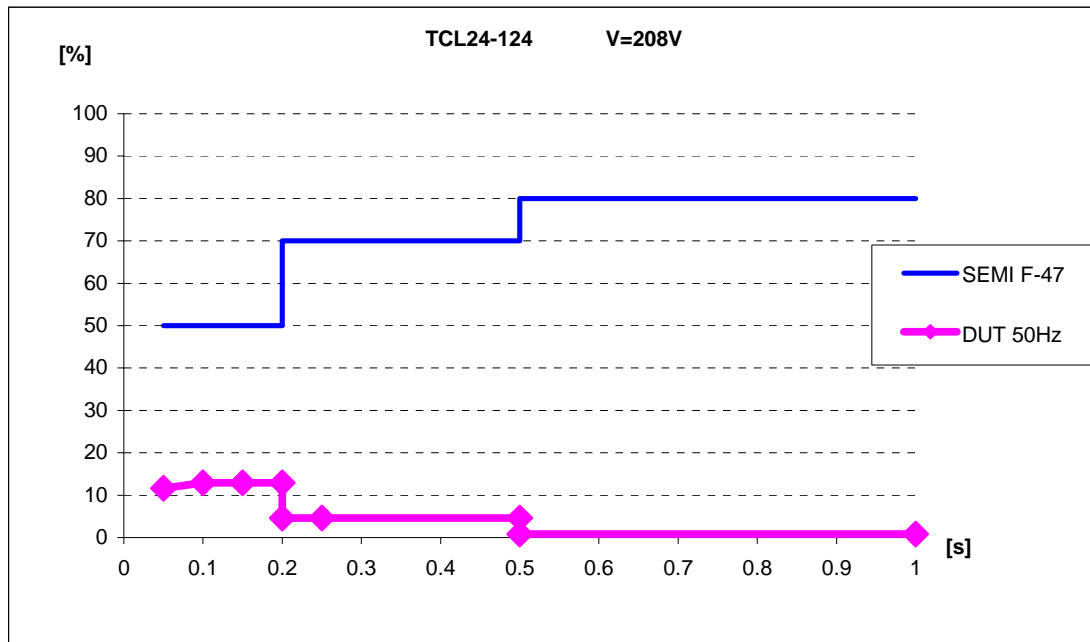
				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
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### 3.3 TCL24-124

Input Voltage V=208VAC

Output: V=24VDC/1.0A

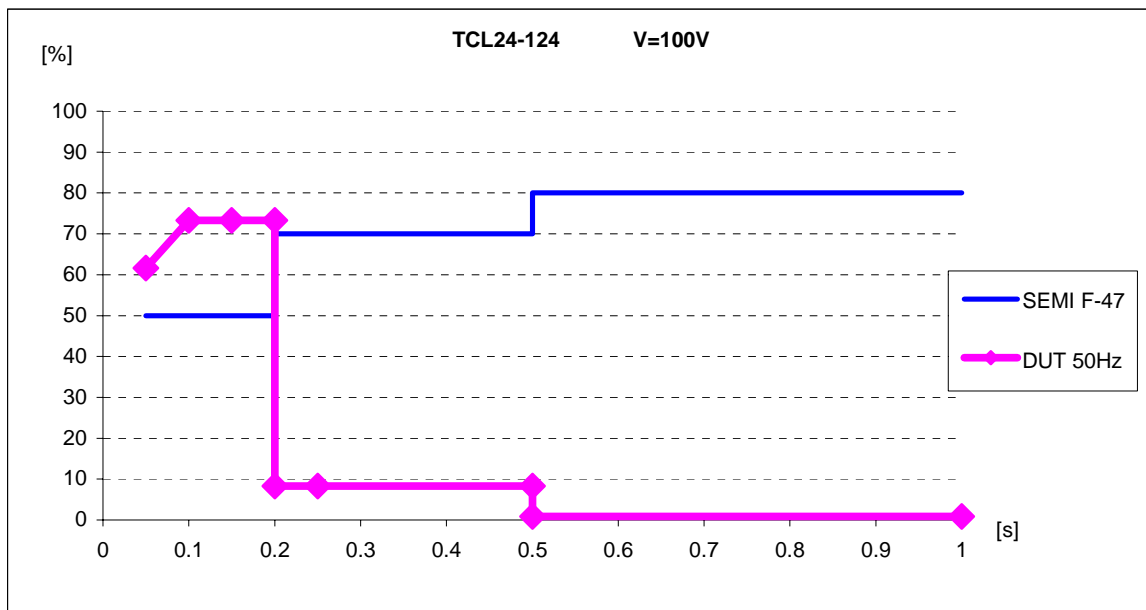
Voltage Sag [V]	Duration		Output Voltage [V]	Percent of Nominal		Result
	[s]	Cycles		DUT 50Hz [%]	SEMI F47 [%]	
166.4	1	50	24	0	80	PASS
166.4	0.5	25	24	0	80	PASS
145.6	0.5	25	24	0	70	PASS
145.6	0.25	12.5	24	0	70	PASS
145.6	0.2	12.5	24	0	70	PASS
104	0.2	10	24	0	50	PASS
104	0.15	7.5	24	0	50	PASS
104	0.1	5	24	0	50	PASS
104	0.05	2.5	24	0	50	PASS
104	0.02	1	24	0	50	PASS
0	0.02	1	24	0	0	PASS



				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
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**TCL24-124**  
**Input Voltage V=100VAC**  
**Output: V=24VDC/1.0A**

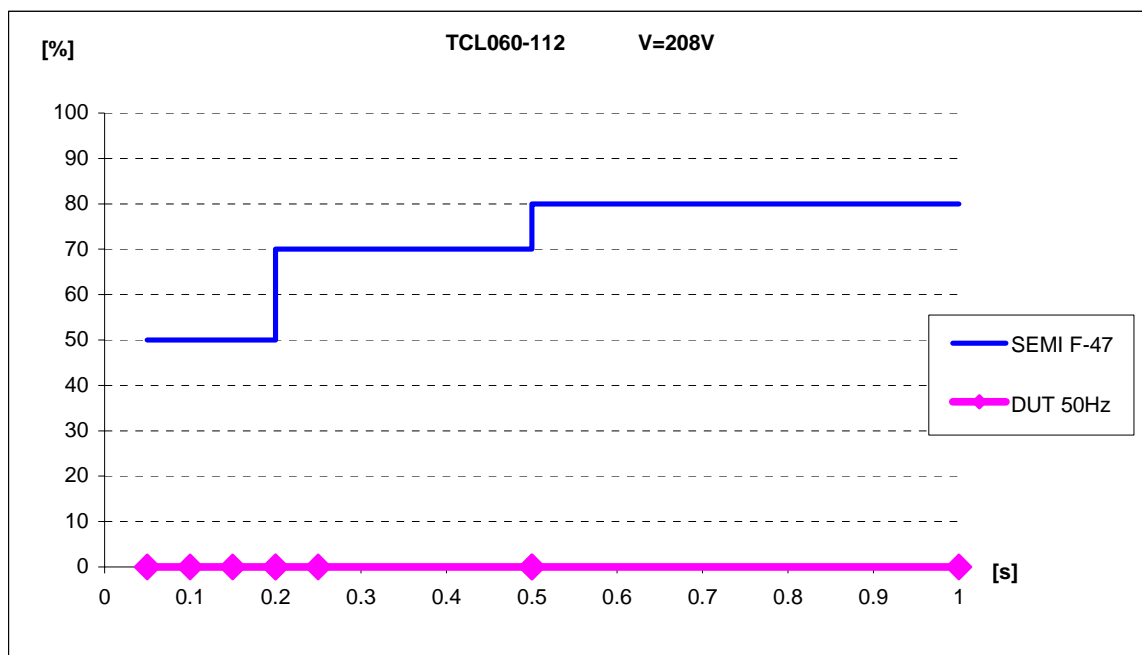
Voltage Sag [V]	Duration [s]	Cycles	Output Voltage [V]	Percent of Nominal		Result
				DUT 50Hz [%]	SEMI F47 [%]	
80	1	50	23.8	0.8	80	PASS
80	0.5	25	23.8	0.8	80	PASS
70	0.5	25	22	8.3	70	PASS
70	0.25	12.5	22	8.3	70	PASS
70	0.2	12.5	22	8.3	70	PASS
50	0.2	10	6.4	73.3	50	FAIL
50	0.15	7.5	6.4	73.3	50	FAIL
50	0.1	5	6.4	73.3	50	FAIL
50	0.05	2.5	9.2	61.7	50	FAIL
50	0.02	1	22	8.3	50	PASS
0	0.02	1	22	8.3	0	PASS



				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
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**3.4 TCL060-112**  
**Input Voltage V=208VAC**  
**Output: V=12VDC/4.0A**

Voltage Sag [V]	Duration		Output Voltage [V]	Percent of Nominal		Result
	[s]	Cycles		DUT 50Hz [%]	SEMI F47 [%]	
166.4	1	50	12	0	80	PASS
166.4	0.5	25	12	0	80	PASS
145.6	0.5	25	12	0	70	PASS
145.6	0.25	12.5	12	0	70	PASS
145.6	0.2	12.5	12	0	70	PASS
104	0.2	10	12	0	50	PASS
104	0.15	7.5	12	0	50	PASS
104	0.1	5	12	0	50	PASS
104	0.05	2.5	12	0	50	PASS
104	0.02	1	12	0	50	PASS
0	0.02	1	12	0	0	PASS

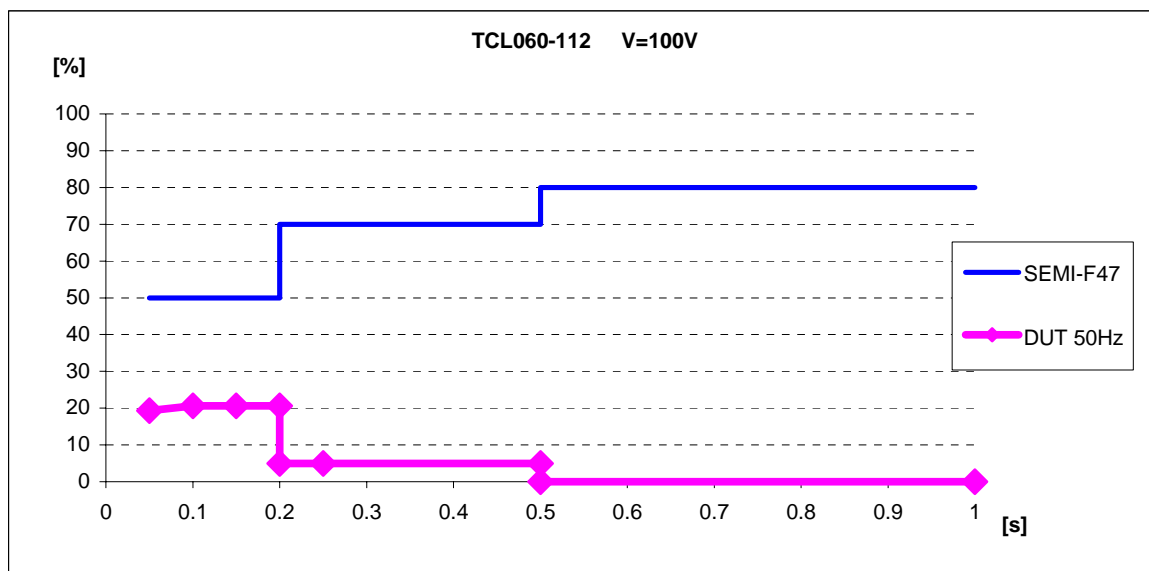


				Date	Name	TEST REPORT TCL SERIES	
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**TCL060-112**  
**Input Voltage V=100VAC**  
**Output: V=12VDC/4.0A**

Voltage Sag [V]	Duration [s]	Cycles	Output Voltage [V]	Percent of Nominal		Result
				DUT 50Hz [%]	SEMI F47 [%]	
80	1	50	12	0	80	PASS
80	0.5	25	12	0	80	PASS
70	0.5	25	11.4	5	70	PASS
70	0.25	12.5	11.4	5	70	PASS
70	0.2	12.5	11.4	5	70	PASS
50	0.2	10	9.52	20.7	50	PASS
50	0.15	7.5	9.52	20.7	50	PASS
50	0.1	5	9.52	20.7	50	PASS
50	0.05	2.5	9.68	19.3	50	PASS
50	0.02	1	12	0	50	PASS
0	0.02	1	12	0	0	PASS



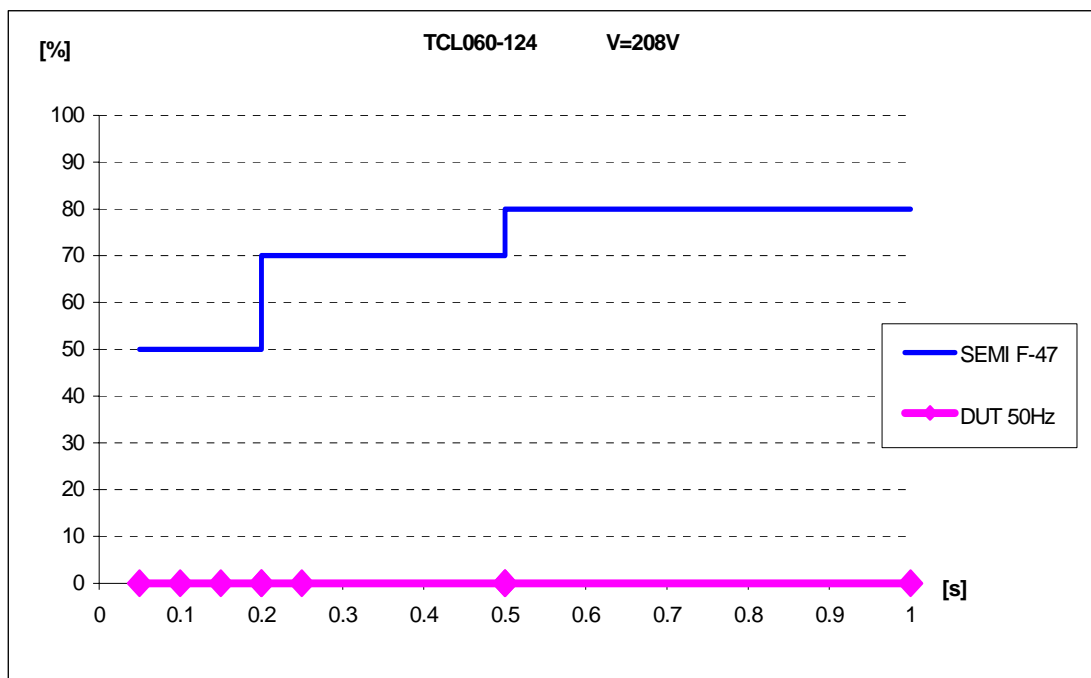
				Date	Name	TEST REPORT TCL SERIES	
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### 3.5 TCL060-124

Input Voltage V=208VAC

Output: V=24VDC/2.5A

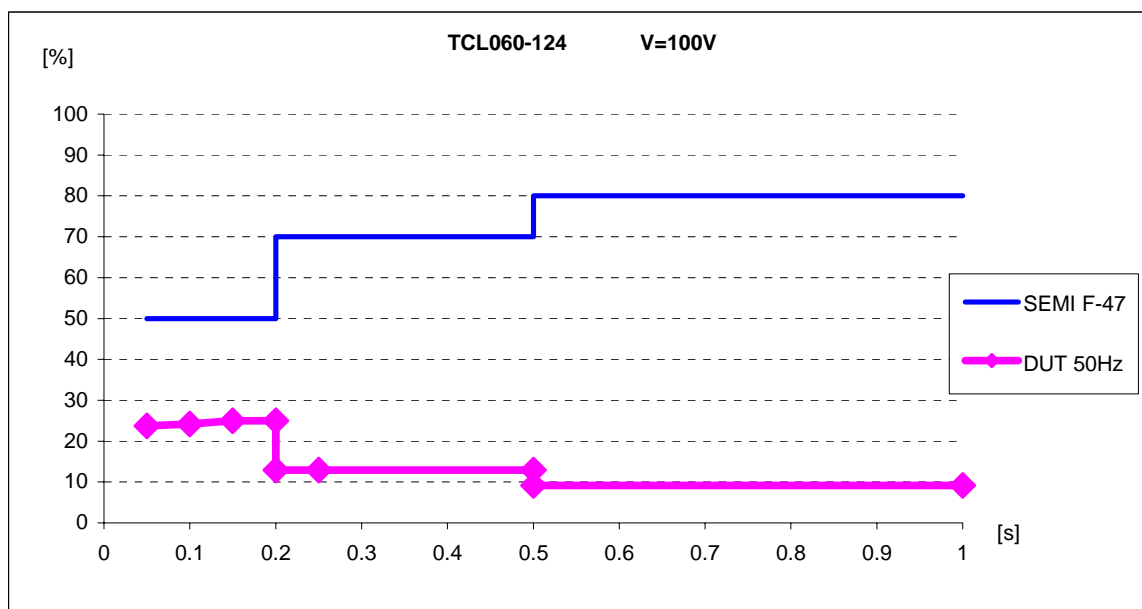
Voltage Sag [V]	Duration		Output Voltage [V]	Percent of Nominal		Result
	[s]	Cycles		DUT 50Hz [%]	SEMI F47 [%]	
166.4	1	50	24.0	0.0	80	PASS
166.4	0.5	25	24.0	0.0	80	PASS
145.6	0.5	25	24.0	0.0	70	PASS
145.6	0.25	12.5	24.0	0.0	70	PASS
145.6	0.2	12.5	24.0	0.0	70	PASS
104	0.2	10	24.0	0.0	50	PASS
104	0.15	7.5	24.0	0.0	50	PASS
104	0.1	5	24.0	0.0	50	PASS
104	0.05	2.5	24.0	0.0	50	PASS
104	0.02	1	24.0	0.0	50	PASS
0	0.02	1	24.0	0.0	0	PASS



				Date	Name	TEST REPORT TCL SERIES	
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**TCL060-124**  
**Input Voltage V=100VAC**  
**Output: V=24VDC/2.5A**

Voltage Sag [V]	Duration [s]	Cycles	Output Voltage [V]	Percent of Nominal		Result
				DUT 50Hz [%]	SEMI F47 [%]	
80	1	50	21.8	9.2	80	PASS
80	0.5	25	21.8	9.2	80	PASS
70	0.5	25	20.9	12.9	70	PASS
70	0.25	12.5	20.9	12.9	70	PASS
70	0.2	12.5	20.9	12.9	70	PASS
50	0.2	10	18	25	50	PASS
50	0.15	7.5	18	25	50	PASS
50	0.1	5	18.2	24.2	50	PASS
50	0.05	2.5	18.3	23.8	50	PASS
50	0.02	1	21.4	10.8	50	PASS
0	0.02	1	21.4	10.8	0	PASS



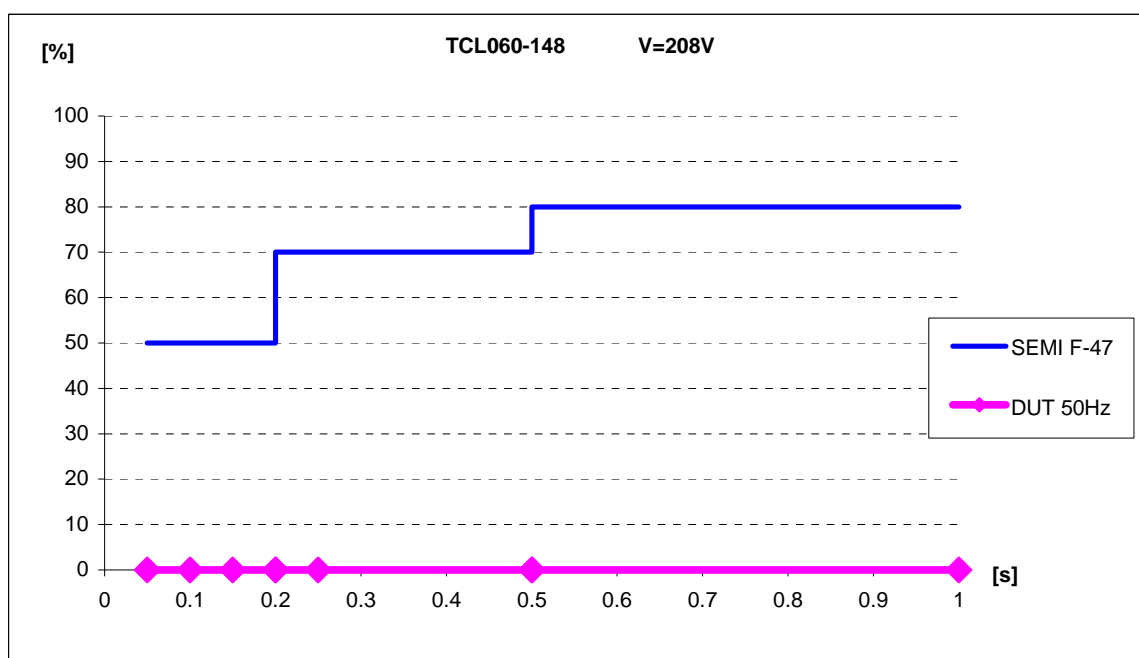
				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
						SEMI F47 Compliance	Sheet/of 11/20
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### 3.6 TCL060-148

Input Voltage V=208VAC

Output: V=48VDC/1.25A

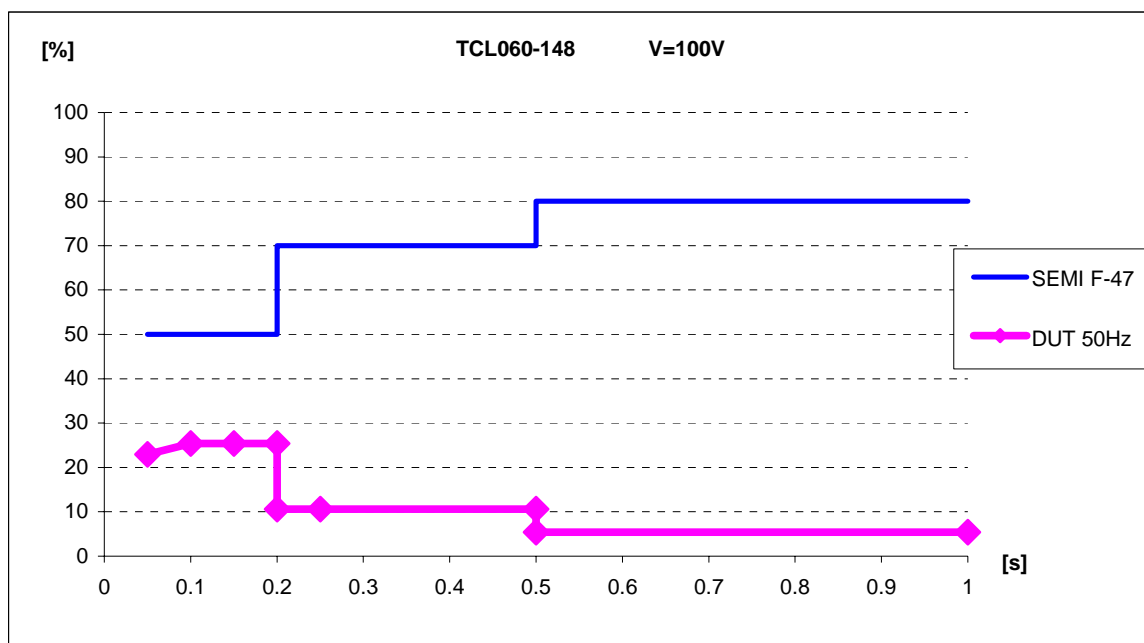
Voltage Sag [V]	Duration		Output Voltage [V]	Percent of Nominal		Result
	[s]	Cycles		DUT 50Hz [%]	SEMI F47 [%]	
166.4	1	50	48	0	80	PASS
166.4	0.5	25	48	0	80	PASS
145.6	0.5	25	48	0	70	PASS
145.6	0.25	12.5	48	0	70	PASS
145.6	0.2	12.5	48	0	70	PASS
104	0.2	10	48	0	50	PASS
104	0.15	7.5	48	0	50	PASS
104	0.1	5	48	0	50	PASS
104	0.05	2.5	48	0	50	PASS
104	0.02	1	48	0	50	PASS
0	0.02	1	48	0	0	PASS



				Date	Name	TEST REPORT TCL SERIES	
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**TCL060-148**  
**Input Voltage V=100VAC**  
**Output: V=48VDC/1.25A**

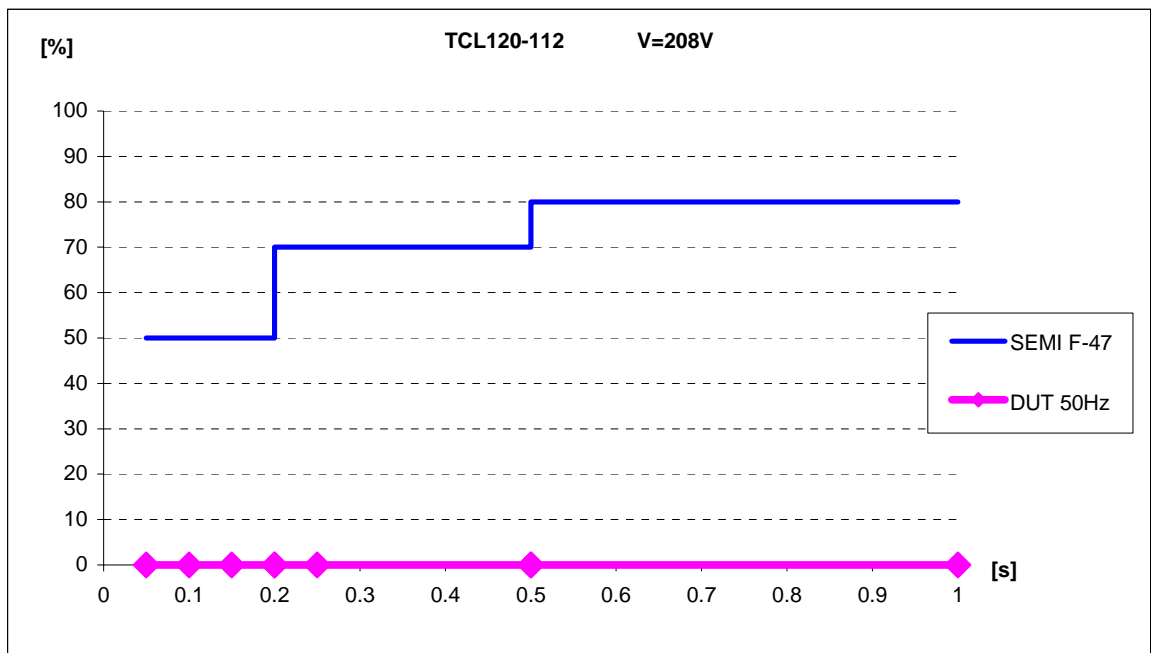
Voltage Sag	Duration		Output Voltage	Percent of Nominal		
[V]	[s]	Cycles	[V]	DUT 50Hz [%]	SEMI F47 [%]	Result
80	1	50	45.4	5.4	80	PASS
80	0.5	25	45.4	5.4	80	PASS
70	0.5	25	42.9	10.6	70	PASS
70	0.25	12.5	42.9	10.6	70	PASS
70	0.2	12.5	42.9	10.6	70	PASS
50	0.2	10	35.8	25.4	50	PASS
50	0.15	7.5	35.8	25.4	50	PASS
50	0.1	5	35.8	25.4	50	PASS
50	0.05	2.5	37	22.9	50	PASS
50	0.02	1	44.3	7.7	50	PASS
0	0.02	1	44.3	7.7	0	PASS



				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
						SEMI F47 Compliance	Sheet/of 13/20
Iss.	Change	Date	Name				

**3.7 TCL120-112**  
**Input Voltage V=208VAC**  
**Output: V=12VDC/8.0A**

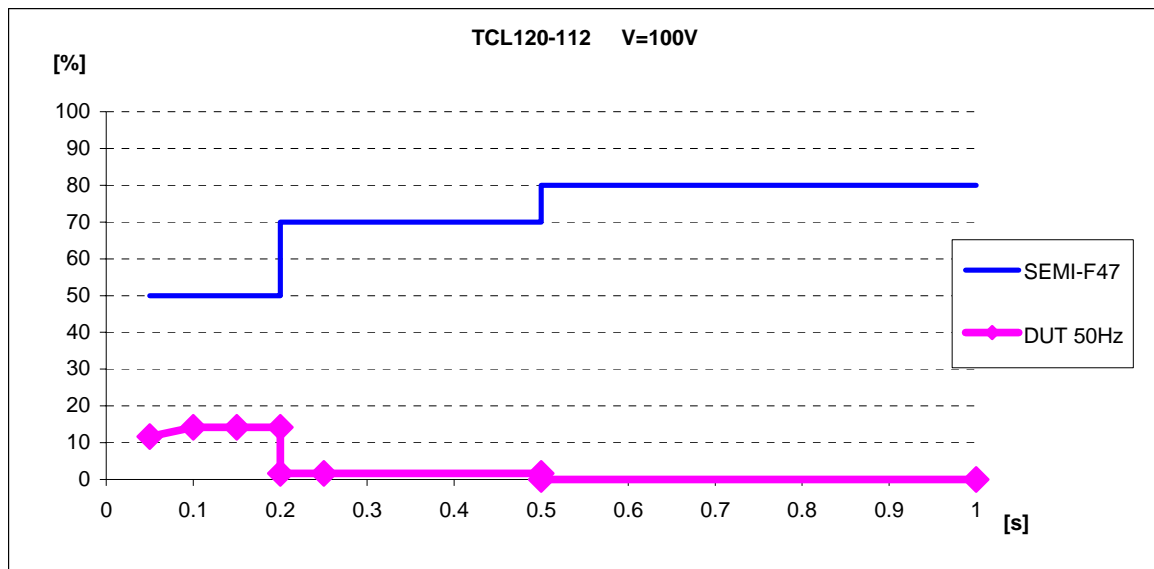
Voltage Sag [V]	Duration		Output Voltage [V]	Percent of Nominal		Result
	[s]	Cycles		DUT 50Hz [%]	SEMI F47 [%]	
166.4	1	50	12	0	80	PASS
166.4	0.5	25	12	0	80	PASS
145.6	0.5	25	12	0	70	PASS
145.6	0.25	12.5	12	0	70	PASS
145.6	0.2	12.5	12	0	70	PASS
104	0.2	10	12	0	50	PASS
104	0.15	7.5	12	0	50	PASS
104	0.1	5	12	0	50	PASS
104	0.05	2.5	12	0	50	PASS
104	0.02	1	12	0	50	PASS
0	0.02	1	12	0	0	PASS



				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
						SEMI F47 Compliance	Sheet/of 14/20
Iss.	Change	Date	Name				

**TCL120-112**  
**Input Voltage V=100VAC**  
**Output: V=12VDC/8.0A**

Voltage Sag [V]	Duration [s]	Cycles	Output Voltage [V]	Percent of Nominal		
				DUT 50Hz [%]	SEMI F47 [%]	Result
80	1	50	12	0	80	PASS
80	0.5	25	12	0	80	PASS
70	0.5	25	11.8	1.7	70	PASS
70	0.25	12.5	11.8	1.7	70	PASS
70	0.2	12.5	11.8	1.7	70	PASS
50	0.2	10	10.3	14.2	50	PASS
50	0.15	7.5	10.3	14.2	50	PASS
50	0.1	5	10.3	14.2	50	PASS
50	0.05	2.5	10.6	11.7	50	PASS
50	0.02	1	12	0	50	PASS
0	0.02	1	12	0	0	PASS



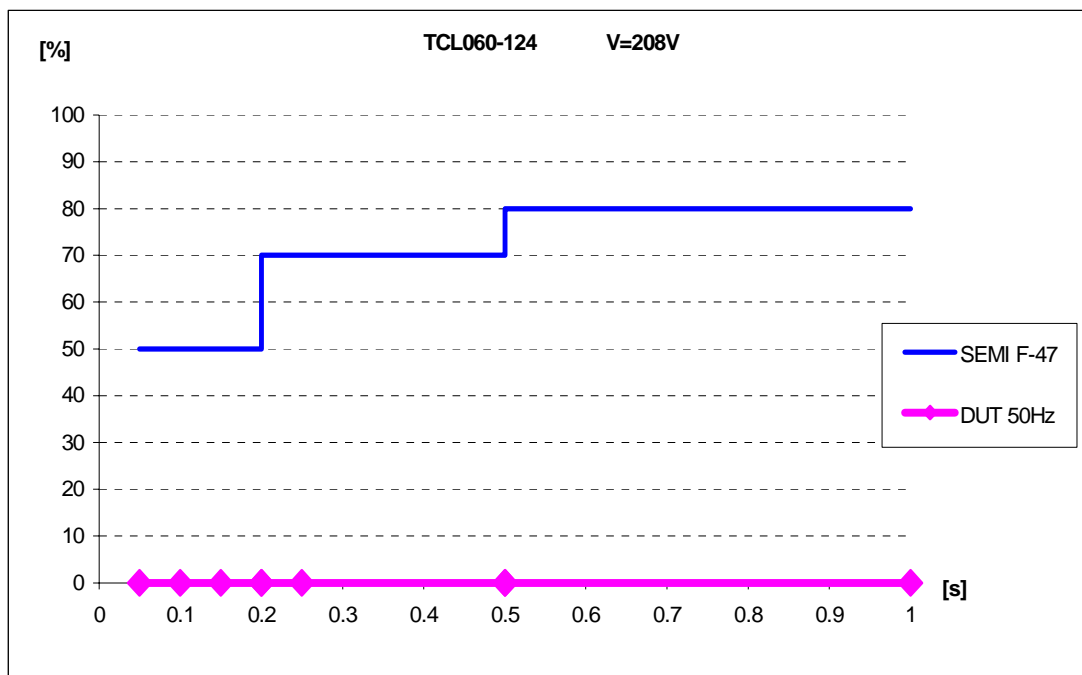
				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
						SEMI F47 Compliance	Sheet/of 15/20
Iss.	Change	Date	Name				

### 3.8 TCL120-124

Input Voltage V=208VAC

Output: V=24VDC/5.0A

Voltage Sag [V]	Duration [s]		Cycles	Output Voltage [V]	Percent of Nominal		Result
					DUT 50Hz [%]	SEMI F47 [%]	
166.4	1	50	24.0	0.0	80		PASS
166.4	0.5	25	24.0	0.0	80		PASS
145.6	0.5	25	24.0	0.0	70		PASS
145.6	0.25	12.5	24.0	0.0	70		PASS
145.6	0.2	12.5	24.0	0.0	70		PASS
104	0.2	10	24.0	0.0	50		PASS
104	0.15	7.5	24.0	0.0	50		PASS
104	0.1	5	24.0	0.0	50		PASS
104	0.05	2.5	24.0	0.0	50		PASS
104	0.02	1	24.0	0.0	50		PASS
0	0.02	1	24.0	0.0	0		PASS

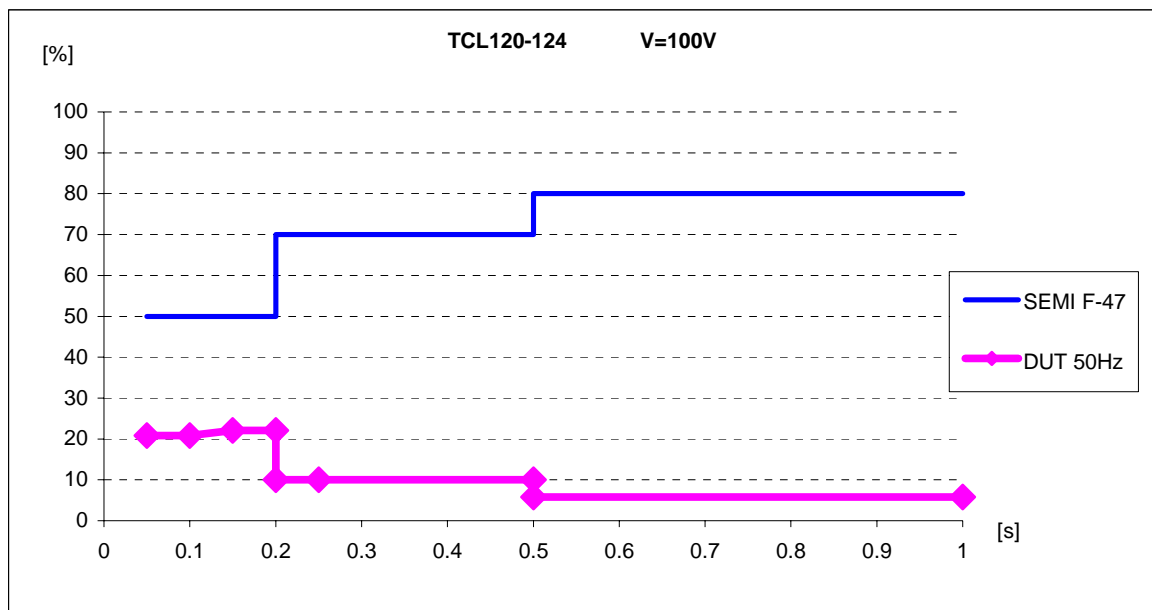


				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
						SEMI F47 Compliance	Sheet/of 16/20
Iss.	Change	Date	Name				



**TCL120-124**  
**Input Voltage V=100VAC**  
**Output: V=24VDC/5.0A**

Voltage Sag	Duration		Output Voltage	Percent of Nominal		
[V]	[s]	Cycles	[V]	DUT 50Hz [%]	SEMI F47 [%]	Result
80	1	50	22.6	5.8	80	PASS
80	0.5	25	22.6	5.8	80	PASS
70	0.5	25	21.6	10	70	PASS
70	0.25	12.5	21.6	10	70	PASS
70	0.2	12.5	21.6	10	70	PASS
50	0.2	10	18.7	22.1	50	PASS
50	0.15	7.5	18.7	22.1	50	PASS
50	0.1	5	19	20.8	50	PASS
50	0.05	2.5	19	20.8	50	PASS
50	0.02	1	22	8.3	50	PASS
0	0.02	1	22	8.3	0	PASS



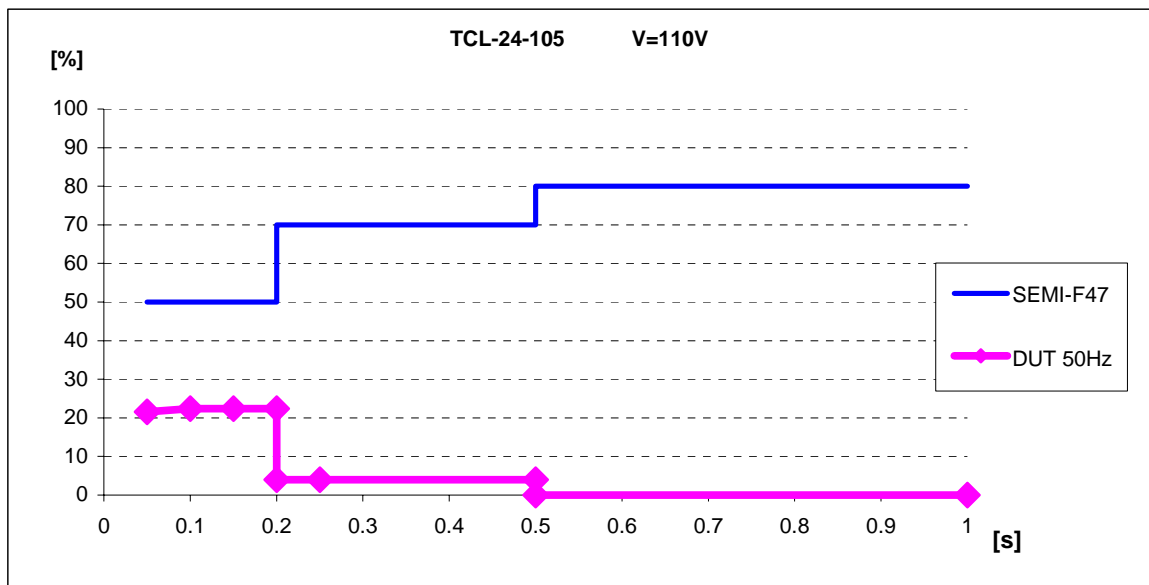
				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
						SEMI F47 Compliance	Sheet/of 17/20
Iss.	Change	Date	Name				

### 3.9 TCL24-105

Input Voltage V=110VAC

Output: V=5VDC/4A

Voltage Sag	Duration		Output Voltage	Percent of Nominal		
[V]	[s]	Cycles	[V]	DUT 50Hz [%]	SEMI F47 [%]	Result
88	1	50	5	0.0	80	PASS
88	0.5	25	5	0.0	80	PASS
77	0.5	25	4.8	4	70	PASS
77	0.25	12.5	4.8	4	70	PASS
77	0.2	12.5	4.8	4	70	PASS
55	0.2	10	3.88	22.4	50	PASS
55	0.15	7.5	3.88	22.4	50	PASS
55	0.1	5	3.88	22.4	50	PASS
55	0.05	2.5	3.92	21.6	50	PASS
55	0.02	1	5	0	50	PASS
0	0.02	1	5	0	0	PASS



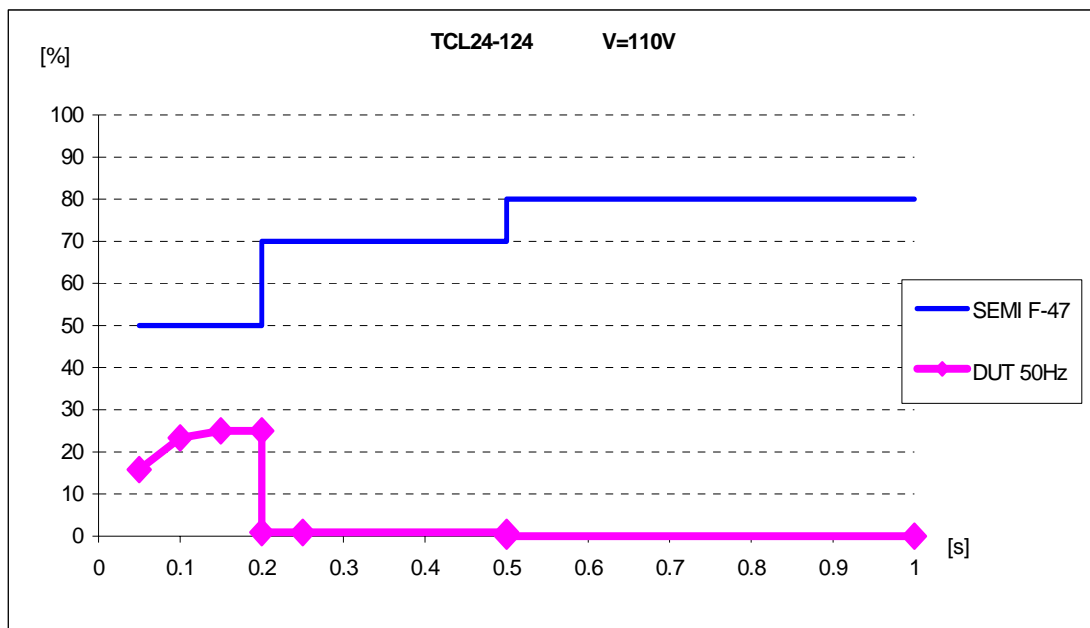
				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
						SEMI F47 Compliance	Sheet/of
							18/20
Iss.	Change	Date	Name				

#### 4.0 TCL24-124

Input Voltage V=110VAC

Output: V=24VDC/1.0A

Voltage Sag [V]	Duration [s]	Cycles	Output Voltage [V]	Percent of Nominal		
				DUT 50Hz [%]	SEMI F47 [%]	Result
88	1	50	24	0	80	PASS
88	0.5	25	24	0	80	PASS
77	0.5	25	23.8	0.8	70	PASS
77	0.25	12.5	23.8	0.8	70	PASS
77	0.2	12.5	23.8	0.8	70	PASS
55	0.2	10	18	25	50	PASS
55	0.15	7.5	18	25	50	PASS
55	0.1	5	18.4	23.3	50	PASS
55	0.05	2.5	20.2	15.8	50	PASS
55	0.02	1	24	0	50	PASS
0	0.02	1	24	0	0	PASS



				Date	Name	TEST REPORT TCL SERIES	
			Prep.	18.05.06	TIM		
						SEMI F47 Compliance	Sheet/of 19/20
Iss.	Change	Date	Name				

## Conclusion

All TCL models where tested at the nominal ranges of 230VAC and 115VAC and the applicable voltage tolerances as per specification. The deviation of the output voltage is noted in the tables (DUT50Hz). All units passed the requirements of the F-47 standard with the restriction to nominal voltage only of the TCL24-105 and TCL24-124. These units will pass the standard at 110VAC input voltage. Details are shown on the last two pages of this report.

					Date	Name	TEST REPORT TCL SERIES	
				Prep.	18.05.06	TIM		
							SEMI F47 Compliance	Sheet/of
								20/20
Iss.	Change	Date	Name					